MRF VME-EVG-230 Driver Development

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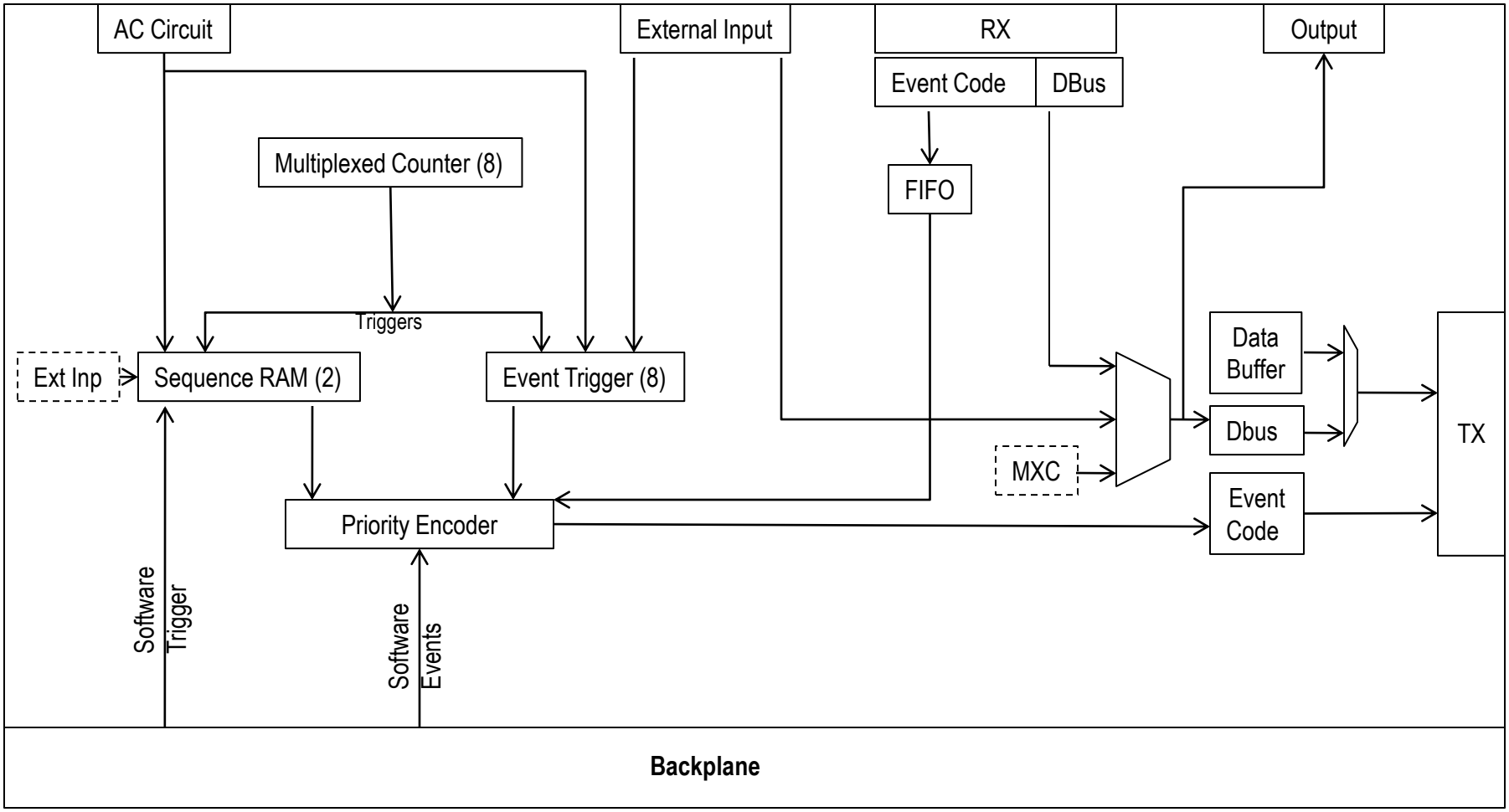
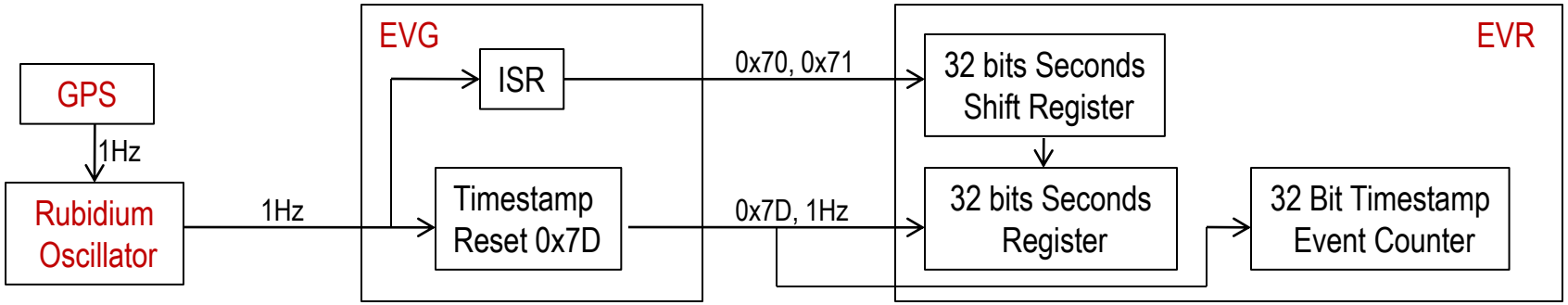
Outline

- EVG Block Diagram
- Timestamping
- Sequencer
- Demo

EVG Block Diagram



Timestamping



- Goal:
  - At the start of every second load the value from shift register into the seconds register and reset the timestamp event counter.
  - Have the next seconds count shifted in the shift register of EVR before the end of the current second.
- Implementation
  - Driver obtains the current time from epicsGeneralTime interface (which inturn is synced to time source) and stores it locally.
  - Every time it gets a pulse from the 1 pps source, driver increments the seconds count of the locally stored time by one.
  - Then it compares the **stored time** with the **current time** obtained from epicsGeneralTime interface.
  - Finally sends out next second using Event Codes 0x70 and 0x71 via software events.
- Advantages
  - Using minimum number of EVG inputs for the timestamping purpose.
- Disadvantages
  - Its software.

Soft and Hard Sequence

- The soft and hard sequences is an abstraction made to separate the process of assembling a sequence from the process of placing it into the hardware.
- The soft sequence contains all the information that is needed to run a sequence in the sequenceRam.
- IOC can have any number of soft sequences but the number of hard sequence is limited by the number of hardware sequenceRam**. This allows us to keep complete, ready to run copy of all sequences in the IOC at all times.**
- The IOC is then free to choose which soft sequence to place into hardware SequenceRam. Since this is a local operation it can be done quickly and efficiently.
- Users do not interact with the sequenceRam directly.
- Modifying the sequence becomes atomic.

Parts of Soft Sequence

- **Event Code List:**

  The list of event codes which will be sent when the sequence starts running.

- **Time Stamp List:**

  Each code must have a timeStamp associated with it. Each timeStamp value is the time at which the corresponding event code will be sent out. Timestamps are relative to the start of the sequence (i.e. trigger from the trigger source).

- **Trigger Source:**

  The sequenceRam can be triggered from several sources including software trigger, trigger from multiplexed counter output, or AC mains voltage synchronization logic output.

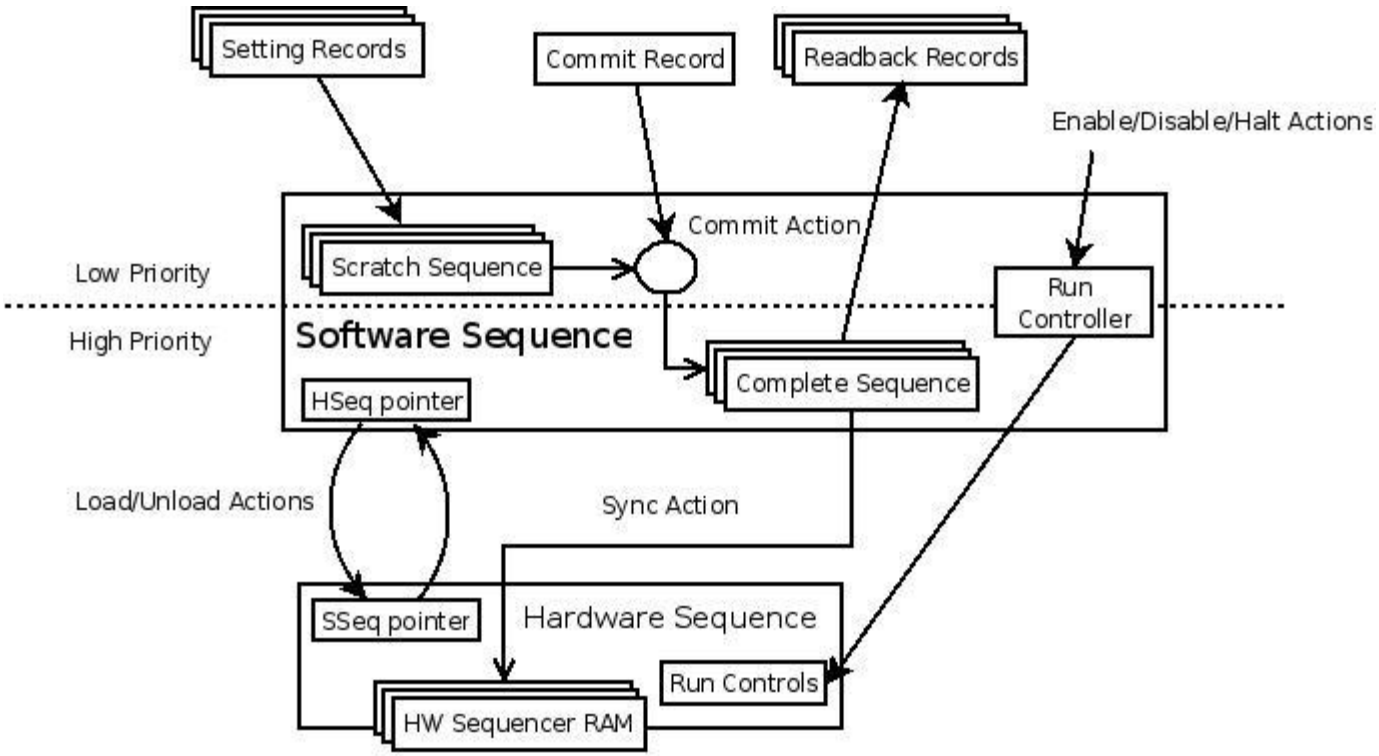
- **Run Mode:**

  Single: When triggered, runs once and then must be manually rearmed.

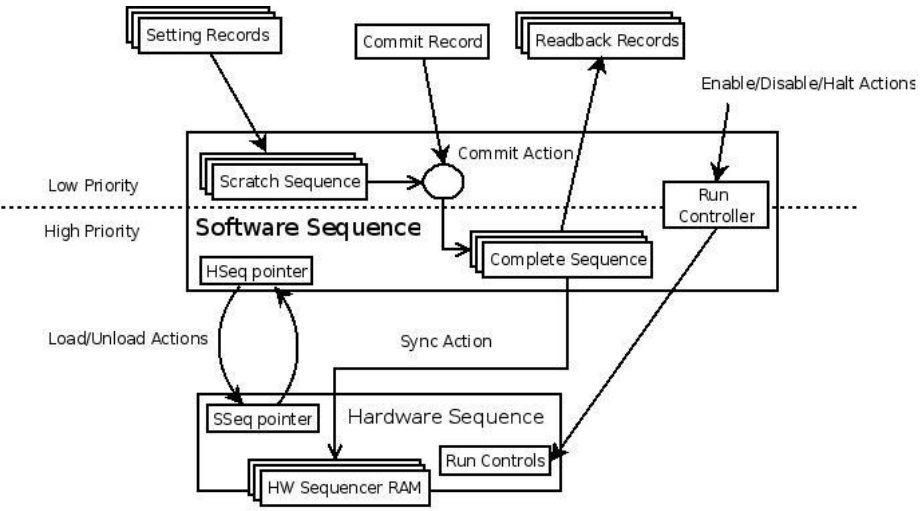
  Normal: Runs when triggered and then automatically rearm.

  Automatic: Runs when triggered and then automatically repeats sequence indefinitely.

Sequence Management Process



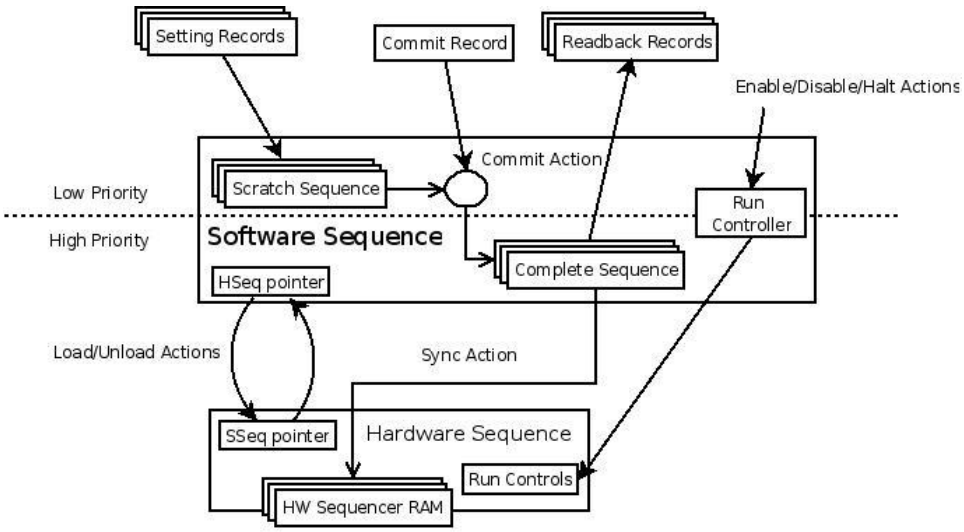
Operations on Soft Sequence



- Load
  - Request that an unassigned hardware sequence be assigned to this soft sequence.
  - This operation will fail if all the sequenceRam are already assigned.
  - If it succeeds the soft sequence becomes loaded.
  - **An allocation scheme ensures that at any given time, each sequenceRam is connected to only one soft sequence.**

  Unload
  - Release the hardware sequence assigned to this soft sequence.
  - This operation can not fail.
  - The soft sequence becomes unloaded.
- Halt:
  - Disables the sequence immediately even if the sequence is running.
  - This action leaves the soft sequence in a disarmed state.

Operations on Soft Sequence (Cont..)



- Commit
  - Cause changes to the scratch sequence to be copied to the complete sequence if the information in scratch sequence is consistent.
  - If the software sequence is loaded then this also initiates a sync action.
  - **It makes sure that the sequenceRam is not modified while it is running**.

Enable:

- Arm a loaded sequence to be triggered.
- This operation can not fail.
- The soft sequence becomes armed.

Disable:

- Take an armed sequence back to a disarmed state.
- This operation can not fail.

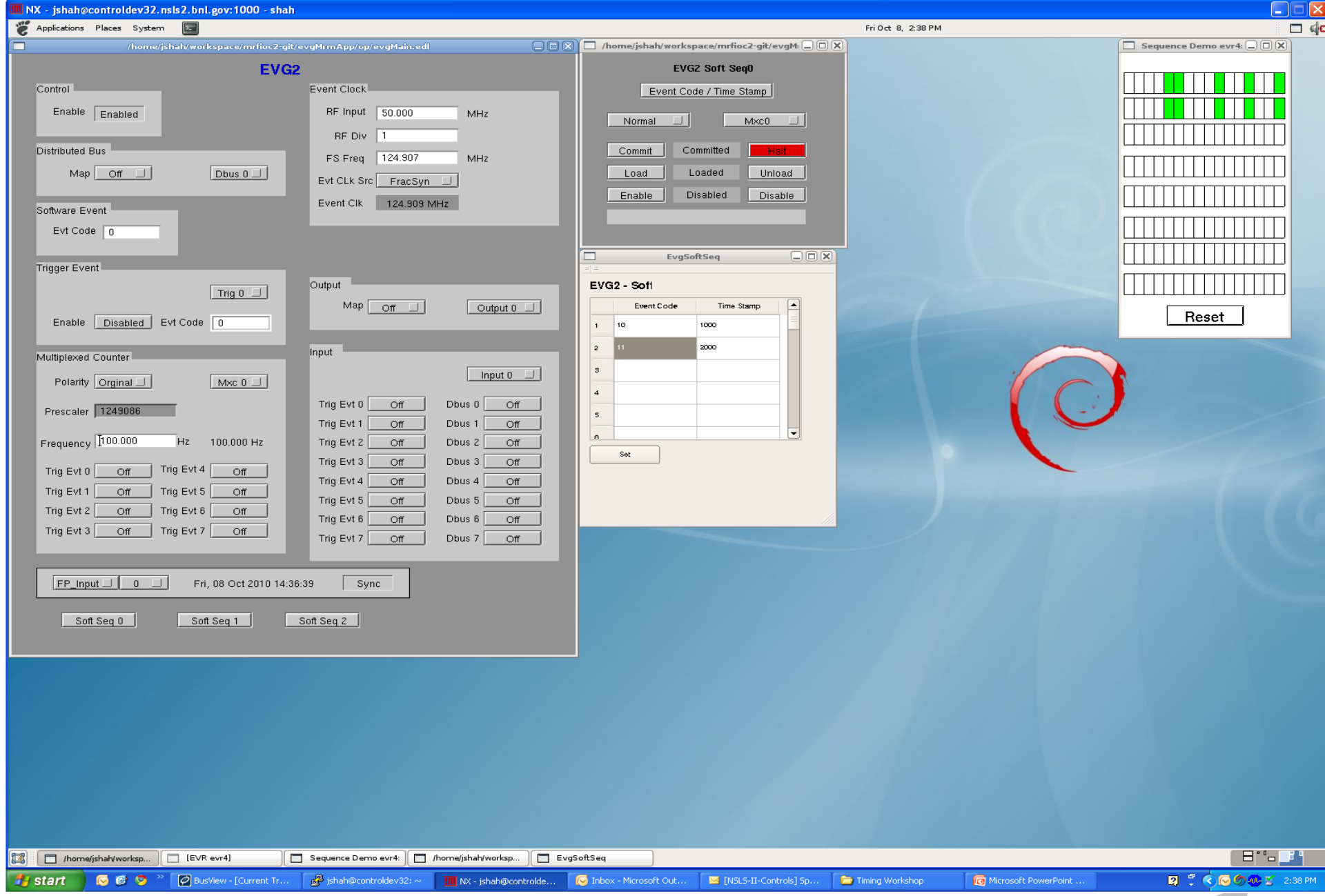
Demo

Acknowledgement

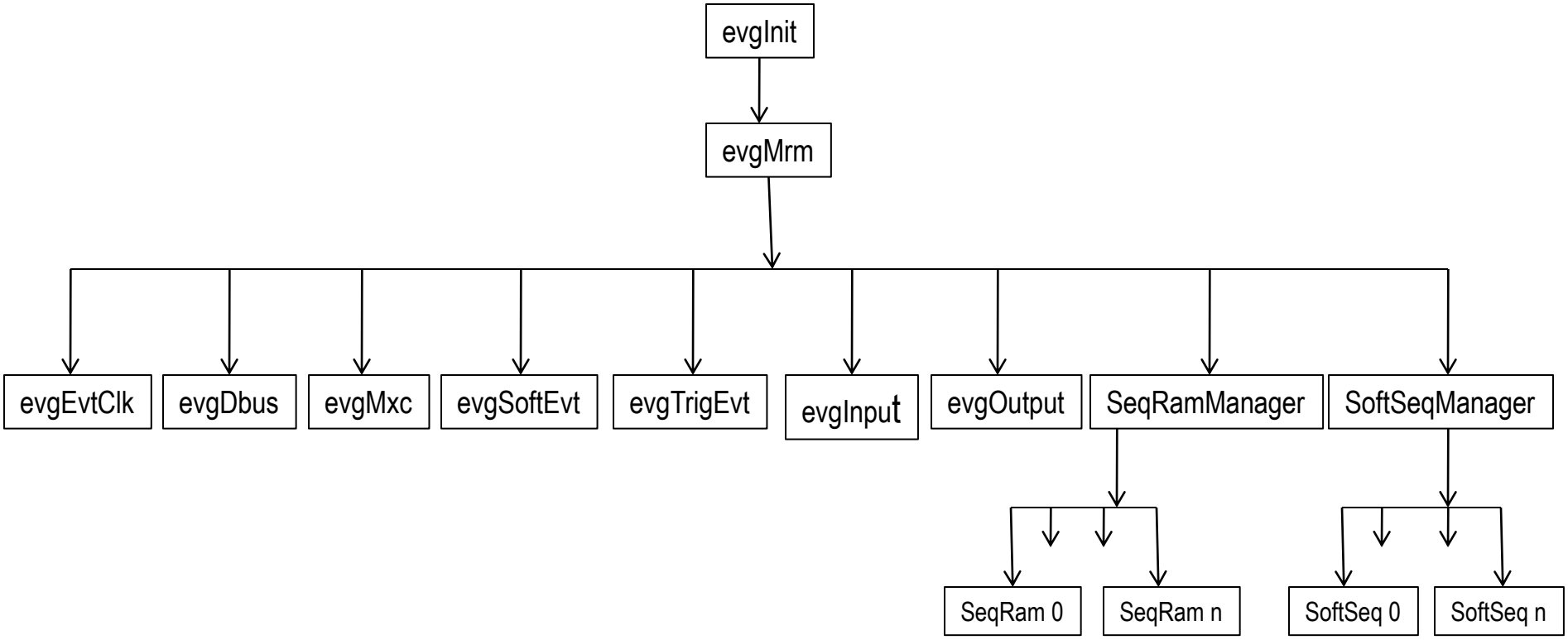
Thanks to

- Michael Davidsaver
- Eric Bjorklund
- Bob Dalesio
- Joseph De Long
- Jukka Pietarinen

Questions…??? Comments…… ???


NX - jshah@controldev32.nsls2.bnl.gov:1000 - shah
Applications Places System
Fri Oct 8, 2:38 PM
/home/jshah/workspace/mrfioc2-git/evgMrmApp/op/evgMain.edl
EVG2
Control
Enable
Enabled
Distributed Bus
Map
Off
Dbus 0
Software Event
Evt Code
0
Trigger Event
Trig 0
Enable
Disabled
Evt Code
0
Multiplexed Counter
Polarity
Orginal
Mxc 0
Prescaler
1249086
Frequency
100.000
Hz
100.000 Hz
Trig Evt 0
Off
Trig Evt 1
Off
Trig Evt 2
Off
Trig Evt 3
Off
Trig Evt 4
Off
Trig Evt 5
Off
Trig Evt 6
Off
Trig Evt 7
Off
Event Clock
RF Input
50.000
MHz
RF Div
1
FS Freq
124.907
MHz
Evt CLk Src
FracSyn
Event Clk
124.909 MHz
Output
Map
Off
Output 0
Input
Input 0
Trig Evt 0
Off
Trig Evt 1
Off
Trig Evt 2
Off
Trig Evt 3
Off
Trig Evt 4
Off
Trig Evt 5
Off
Trig Evt 6
Off
Trig Evt 7
Off
Dbus 0
Off
Dbus 1
Off
Dbus 2
Off
Dbus 3
Off
Dbus 4
Off
Dbus 5
Off
Dbus 6
Off
Dbus 7
Off
FP_Input
0
Fri, 08 Oct 2010 14:36:39
Sync
Soft Seq 0
Soft Seq 1
Soft Seq 2
/home/jshah/workspace/mrfioc2-git/evgM
EVG2 Soft Seq0
Event Code / Time Stamp
Normal
Mxc0
Commit
Committed
Halt
Load
Loaded
Unload
Enable
Disabled
Disable
EvgSoftSeq
EVG2 - Soft
Event Code
Time Stamp
1
10
1000
2
11
2000
3
4
5
6
Set
Sequence Demo evr4:
Reset
/home/jshah/worksp...
[EVR evr4]
Sequence Demo evr4:
/home/jshah/worksp...
EvgSoftSeq
start
BusView - [Current Tr...
jshah@controldev32: ~
NX - jshah@controlde...
Inbox - Microsoft Out...
[NSLS-II-Controls] Sp...
Timing Workshop
Microsoft PowerPoint ...
2:38 PM

Software Layout



Event Source Priority

- Trigger Event 0
- Trigger Event 1
- Trigger Event 2
- Trigger Event 3
- Event Sequencer 1
- Event Sequencer 2 (Super Sequencer Event, under development for the VME-EVG-230)
- Trigger Event 4
- Trigger Event 5
- Trigger Event 6
- Trigger Event 7
- Upstream EVG Event
- SW Event
- Timestamping '0' Event
- Timestamping '1' Event
- Timestamping Second Event